

FIG. 1 (PRIOR ART)

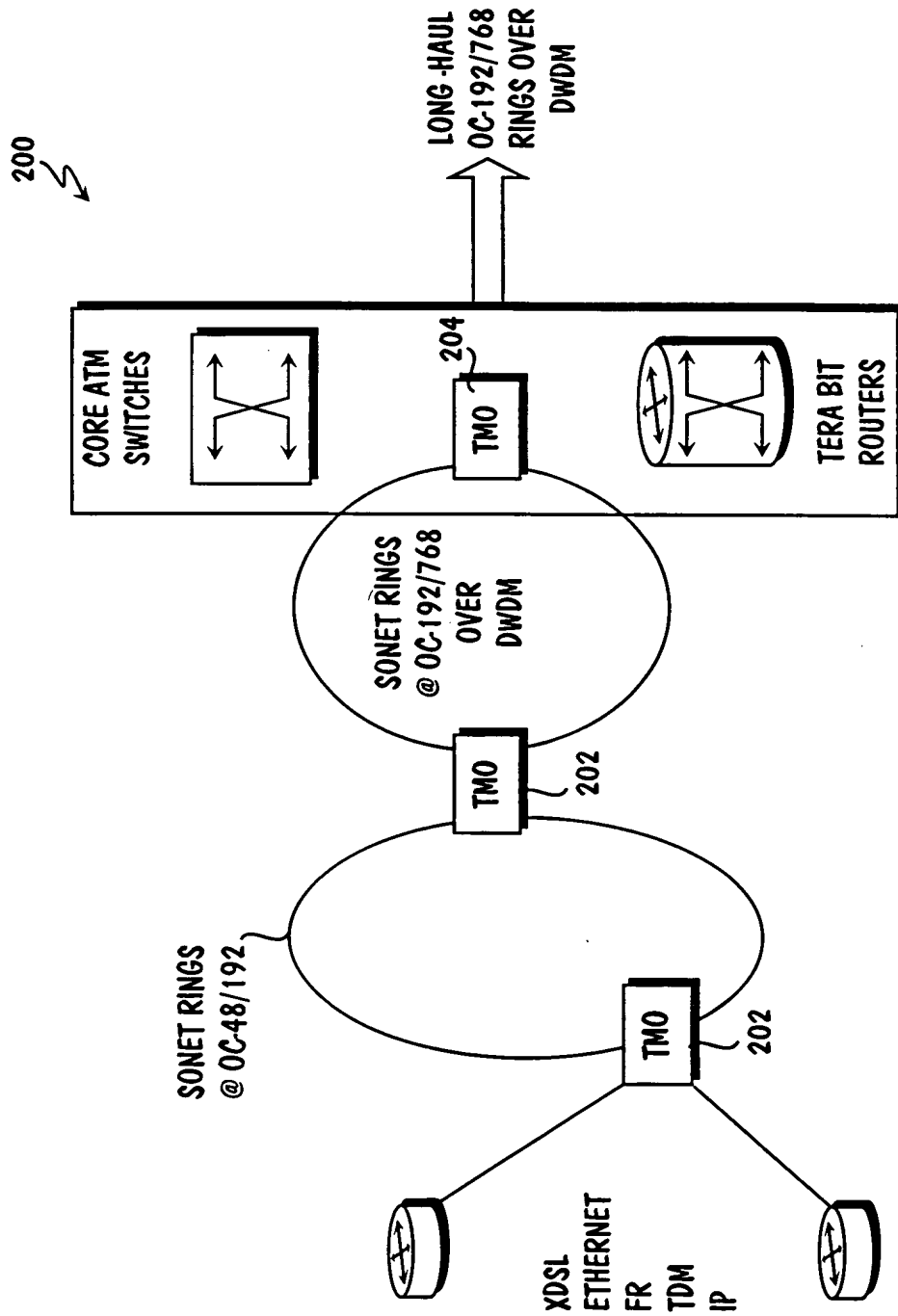


FIG. 2

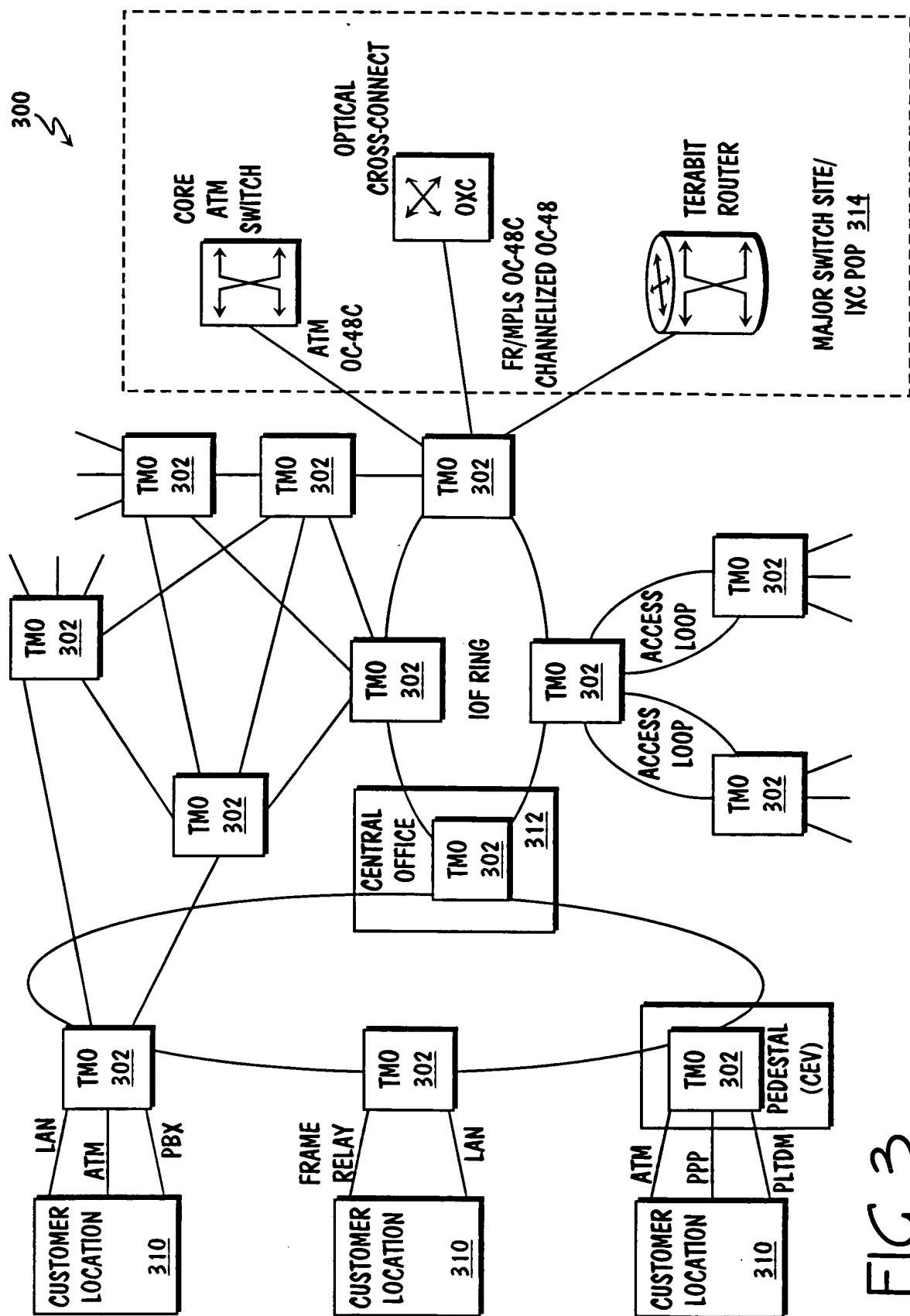


FIG. 3

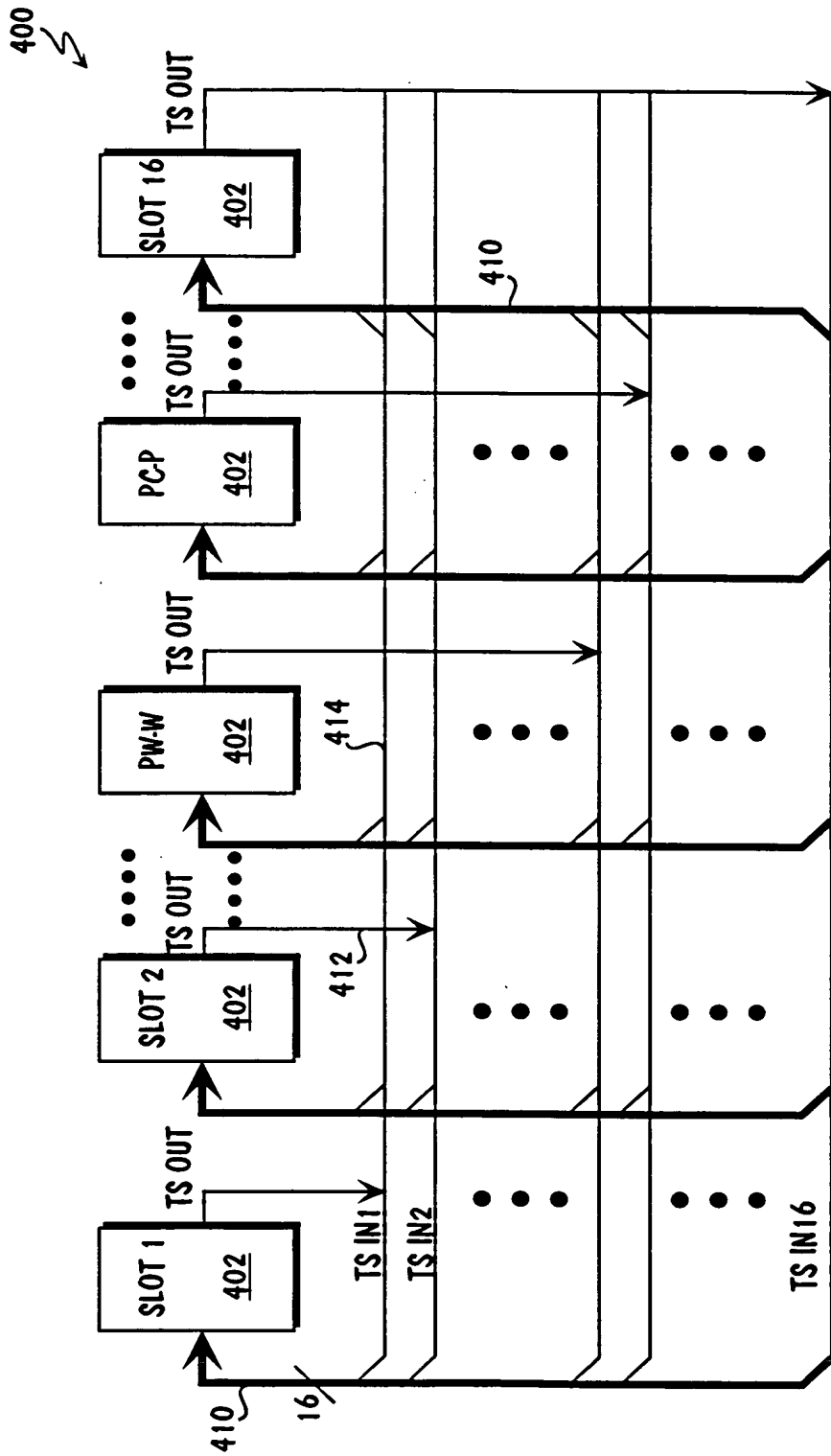


FIG. 4

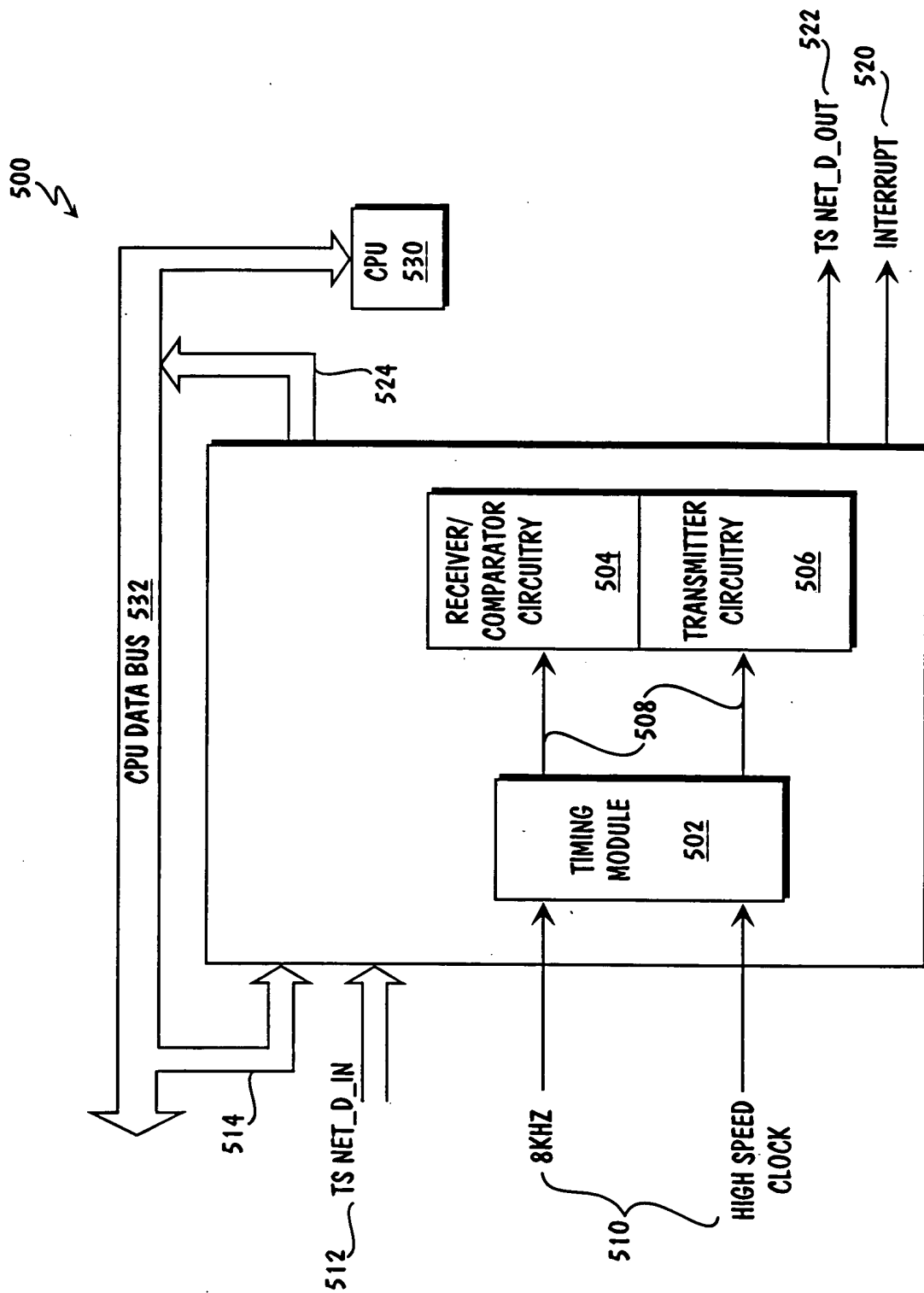


FIG. 5

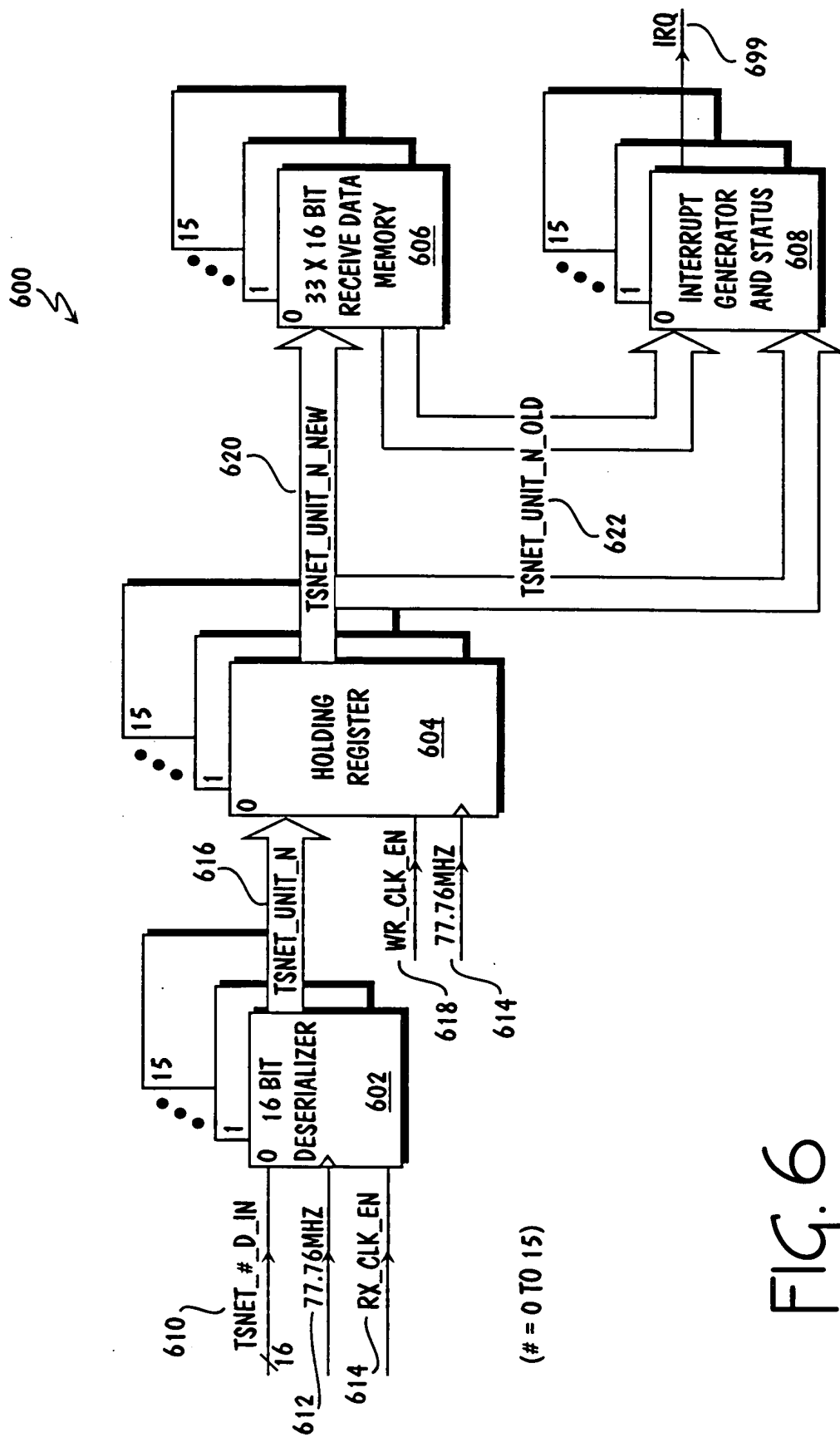


FIG. 6

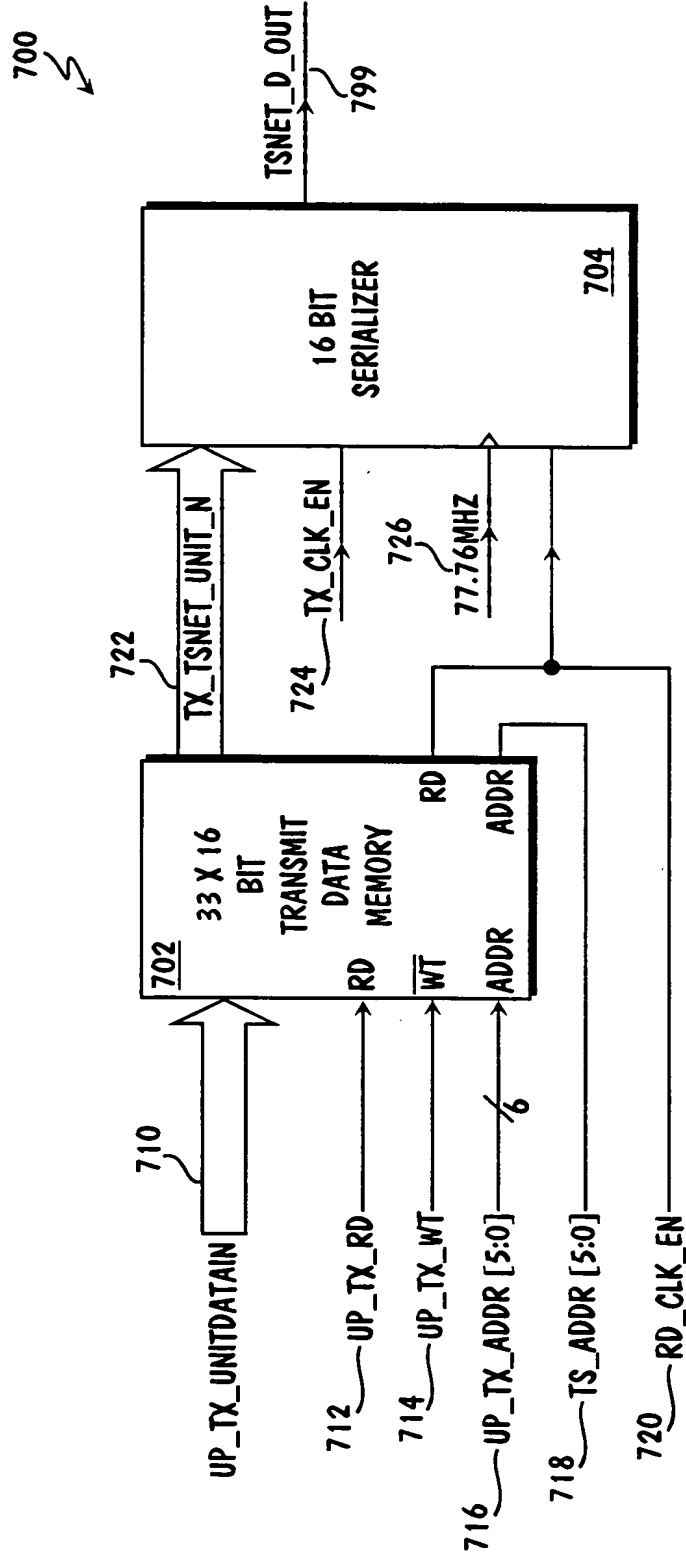


FIG. 7

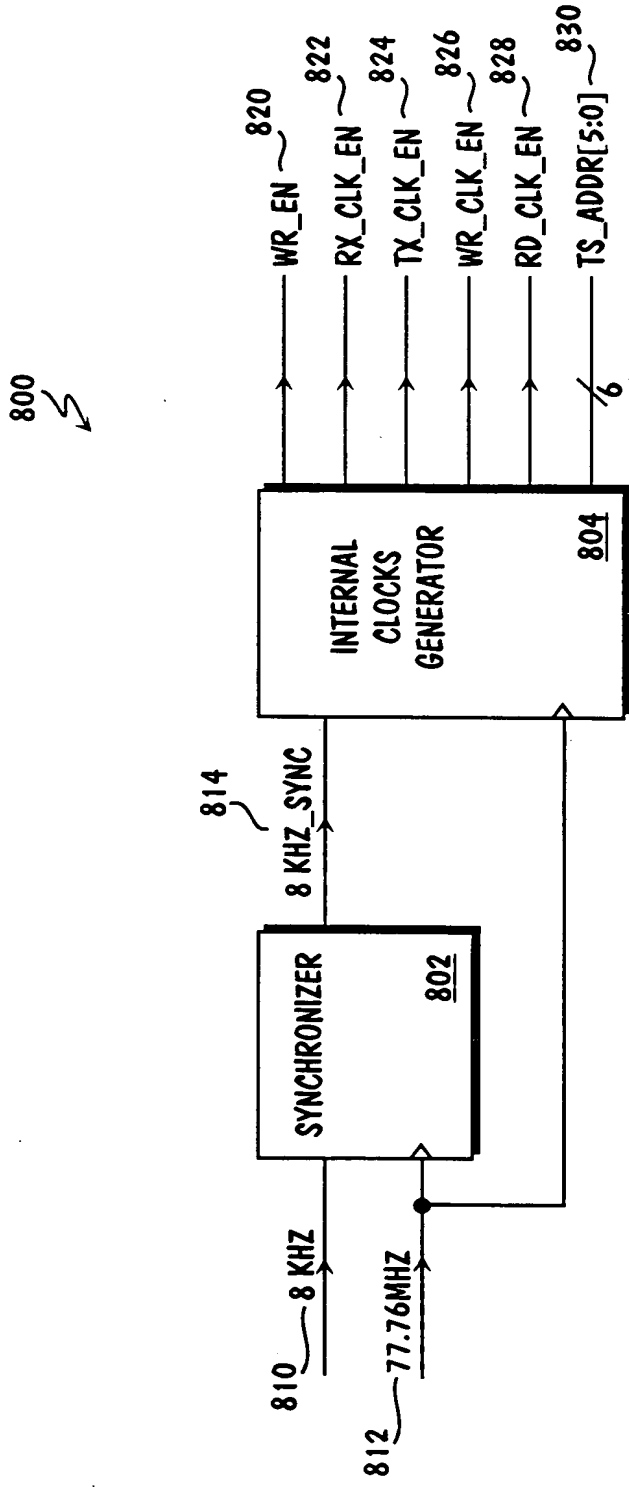


FIG. 8

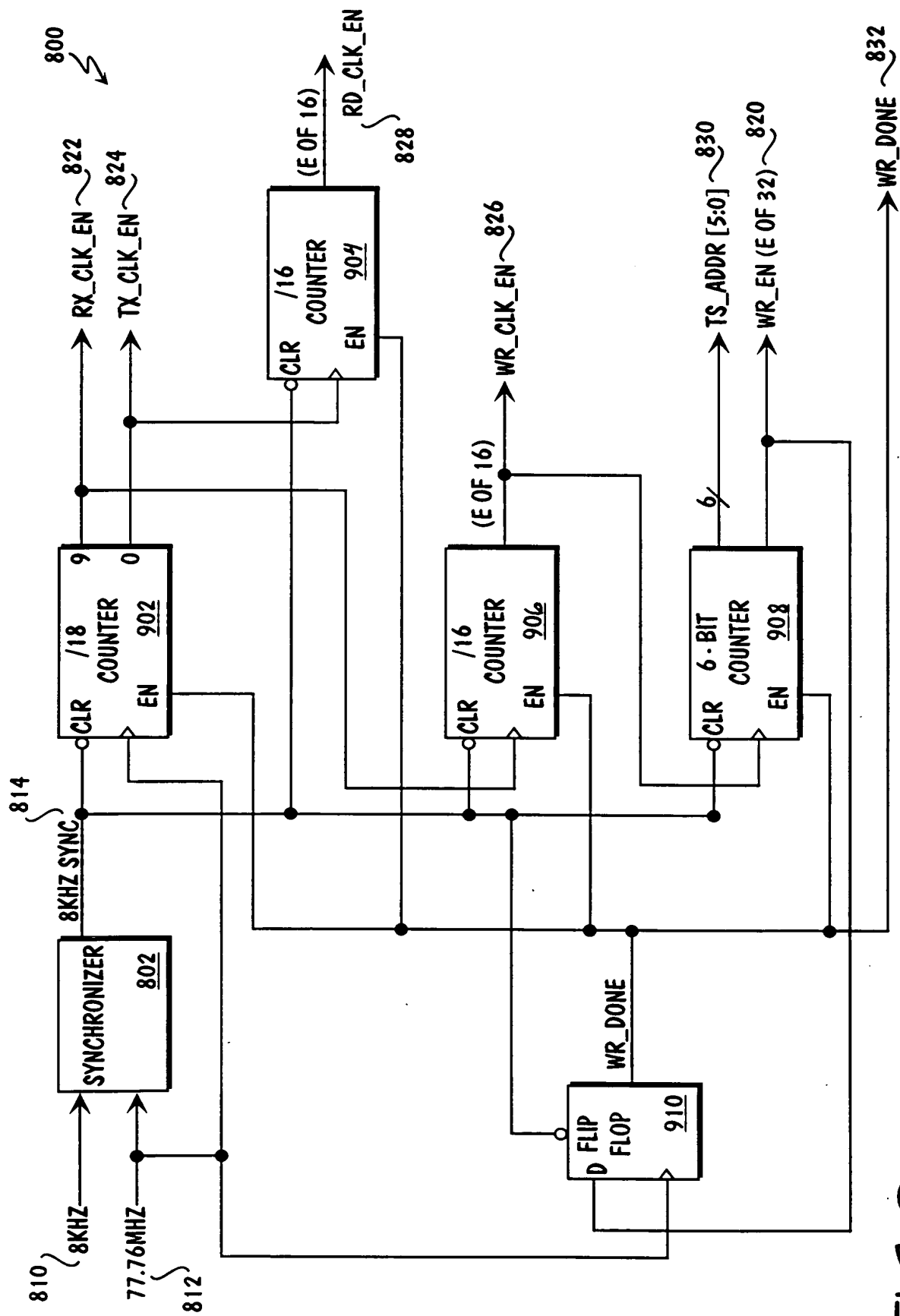


FIG. 9

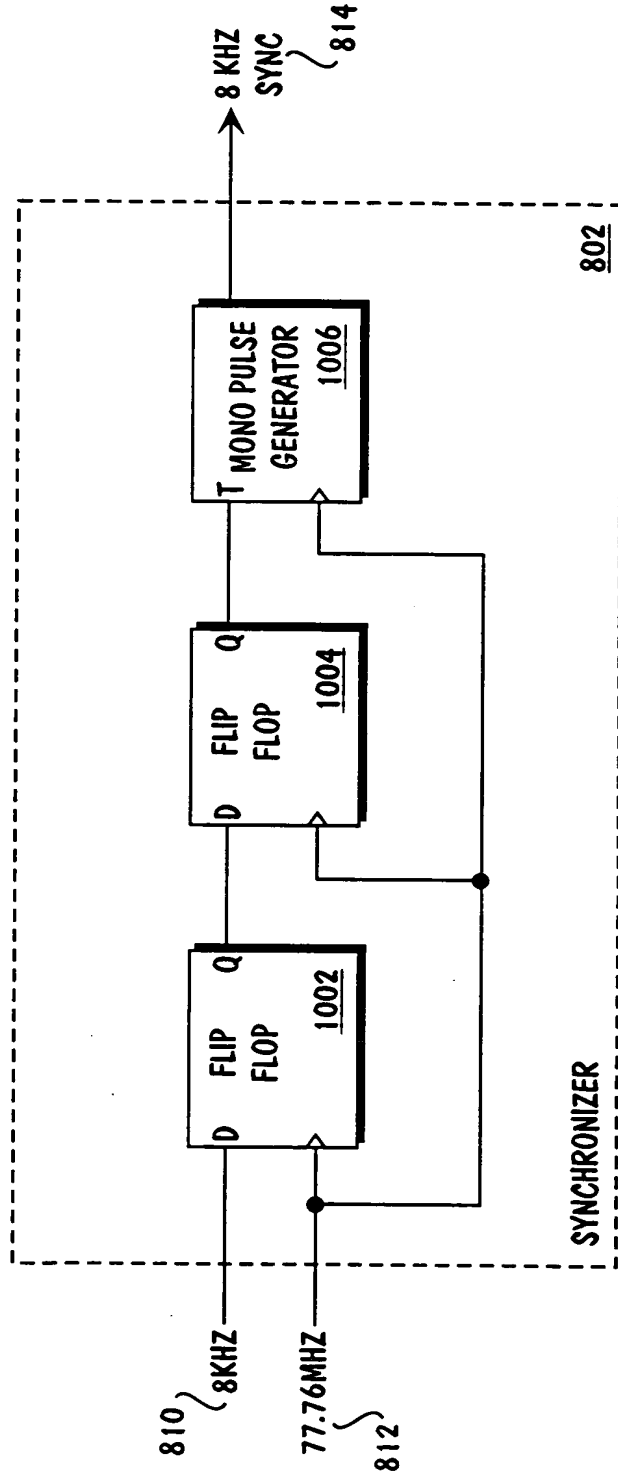


FIG. 10

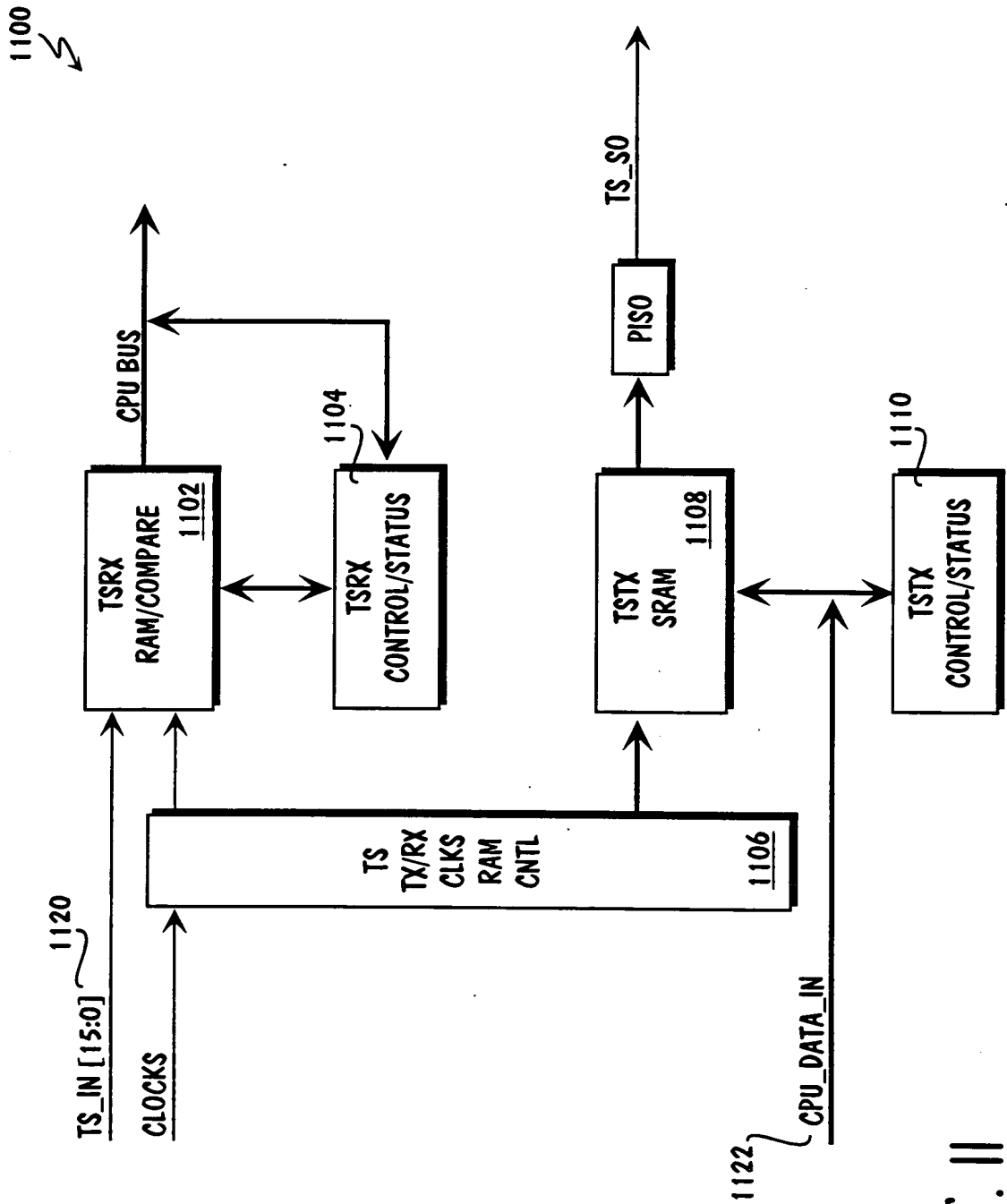


FIG. 11

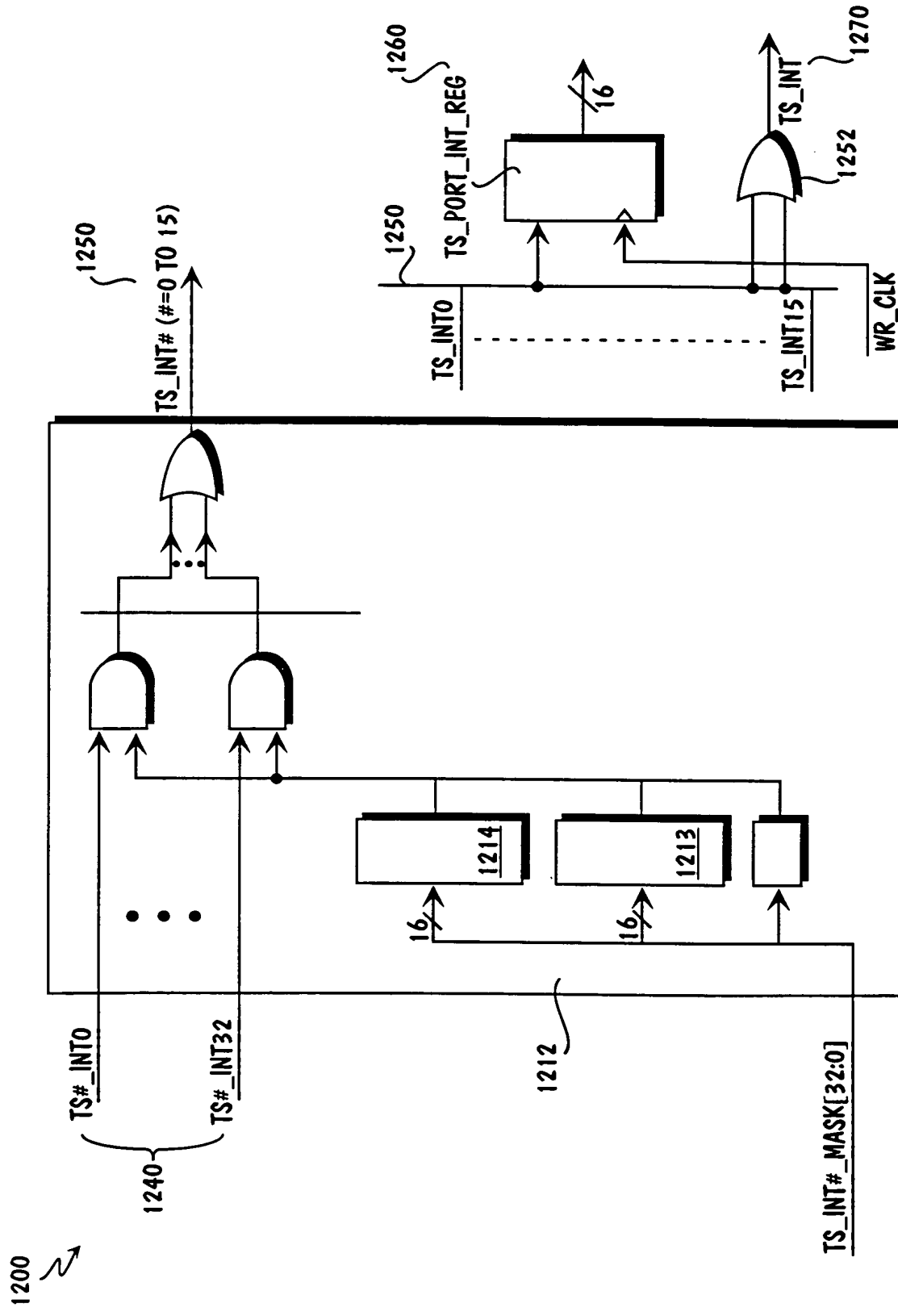


FIG. 12B

1300

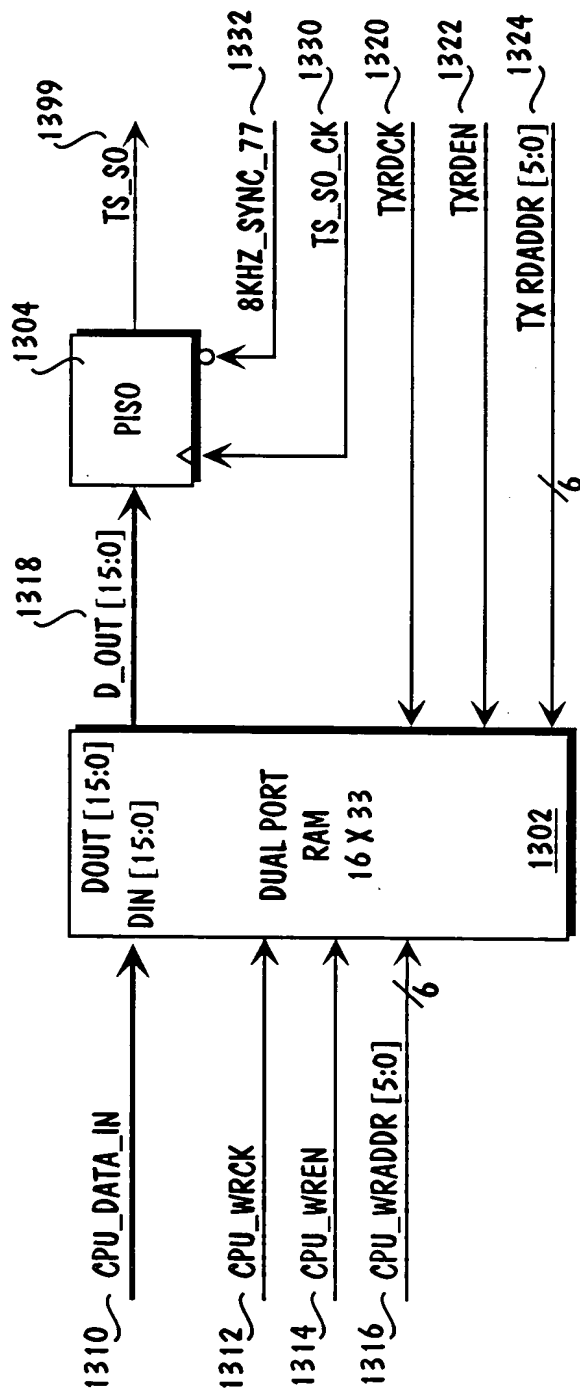


FIG. 13

09662681-091500

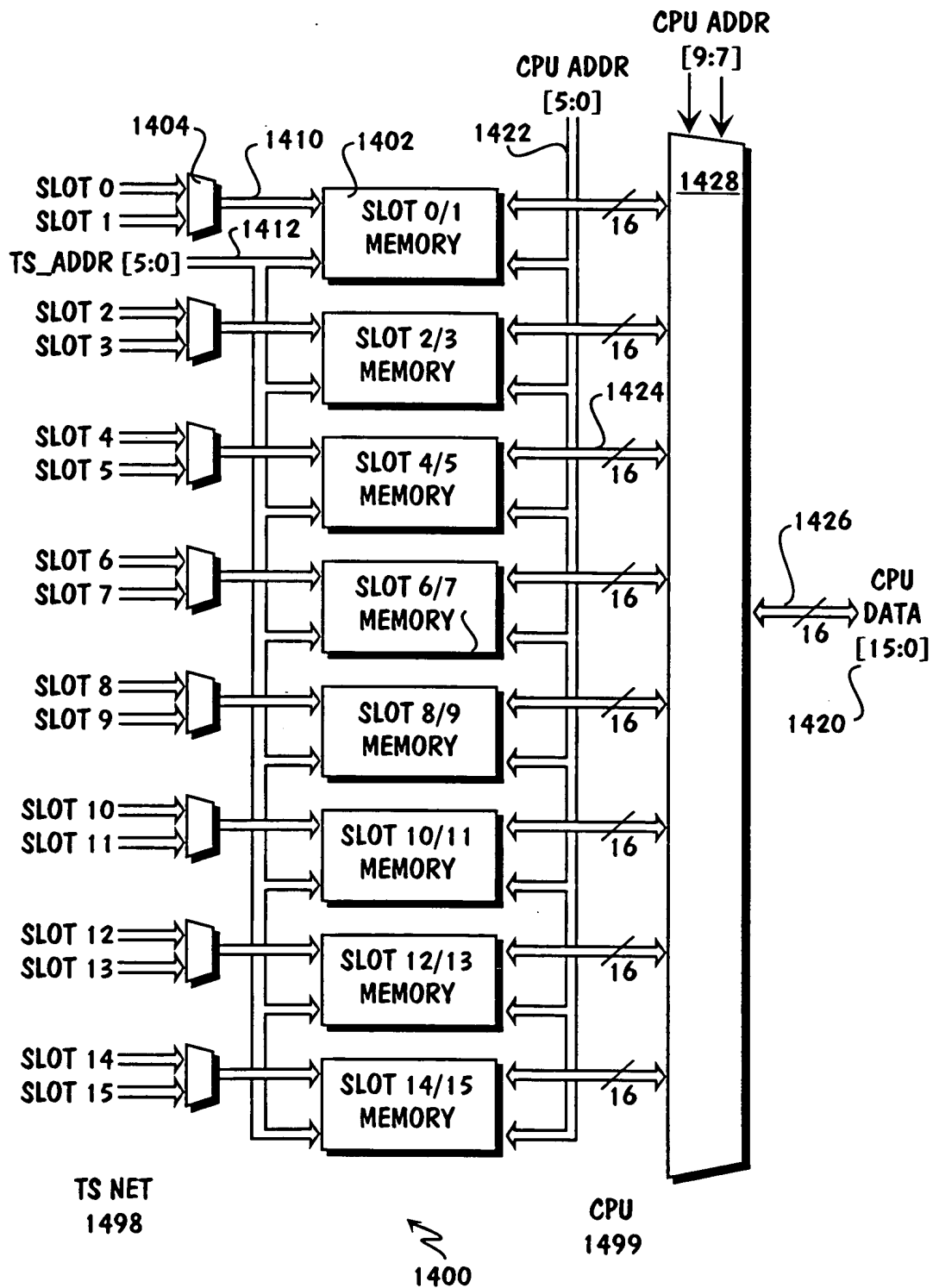


FIG. 14

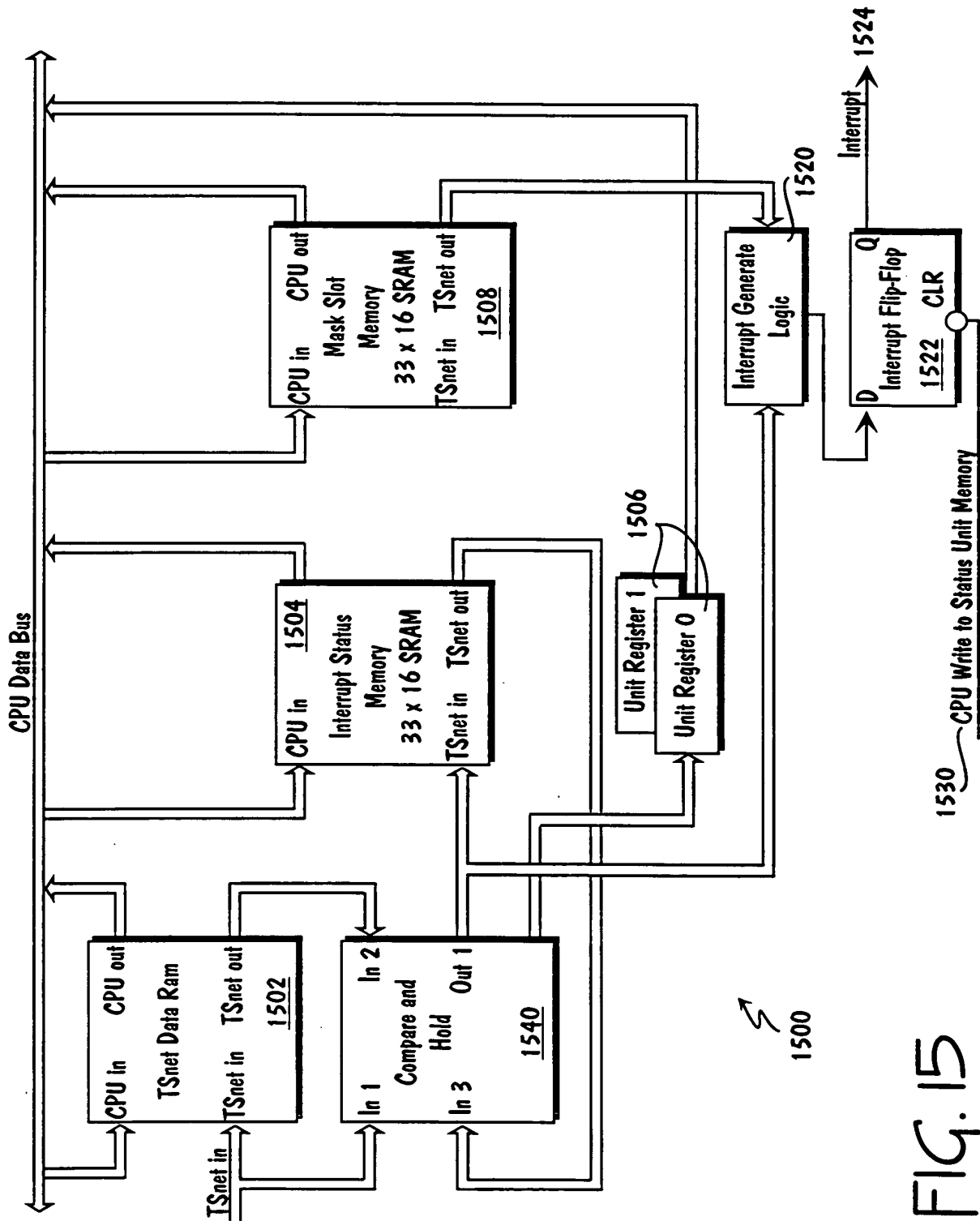


FIG. 15

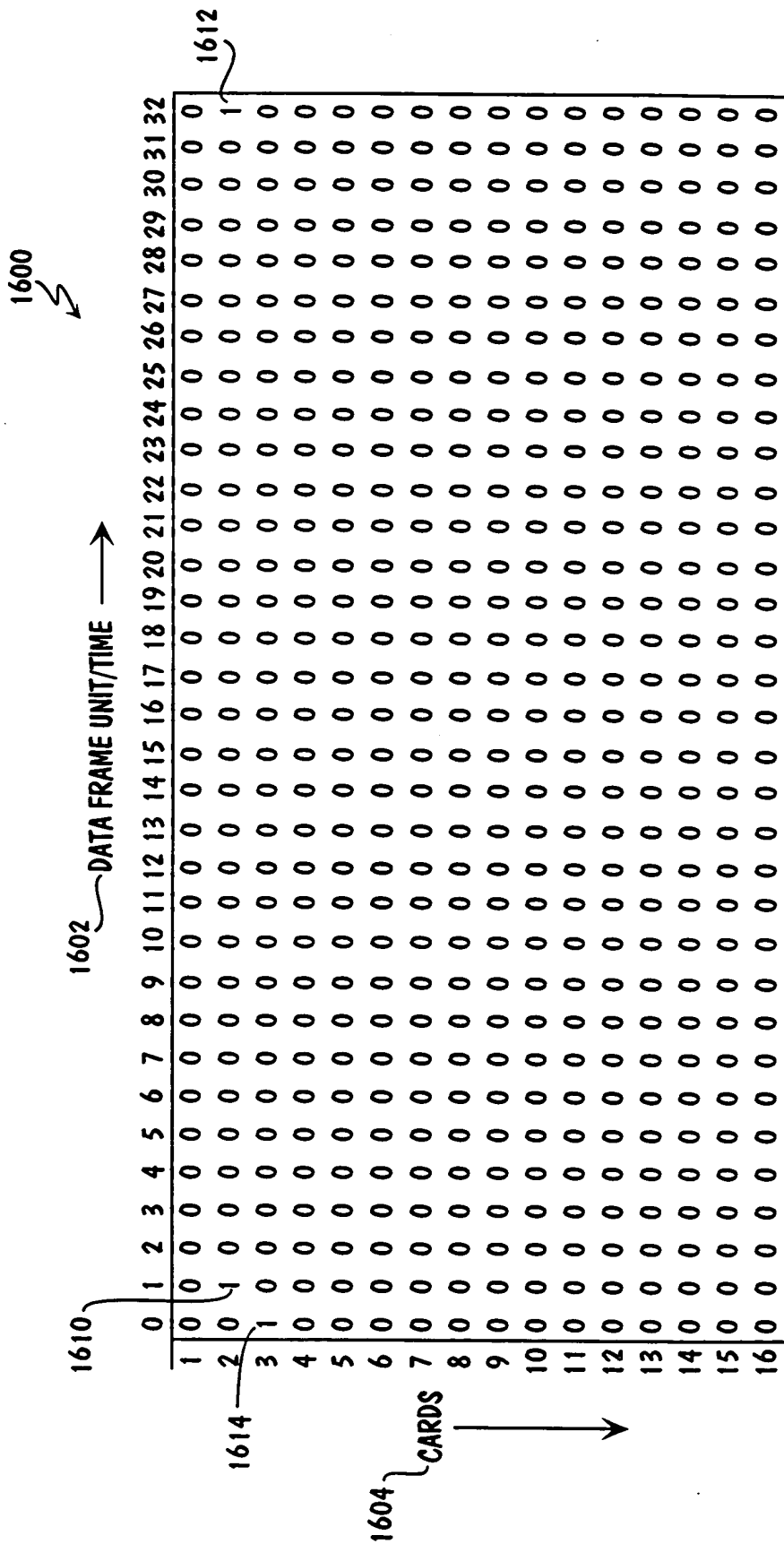


FIG. 16

005T60" T8929960

1800
↘

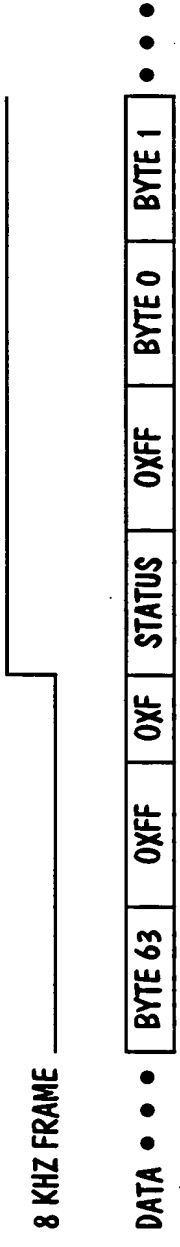


FIG. 18

BIT	7 (MSB)	6	5	4	3	2	1	0 (LSB)
FUNCTION	BRDSTS1	BRDSTS0	1	1	1	1	1	1

STSB1	STSB0	INTERPRETATION
0	0	PRESENT & FAILED (OR NOT BOOTED)
0	1	PRESENT & INACTIVE
1	0	PRESENT & ACTIVE
1	1	NOT PRESENT

FIG. 19

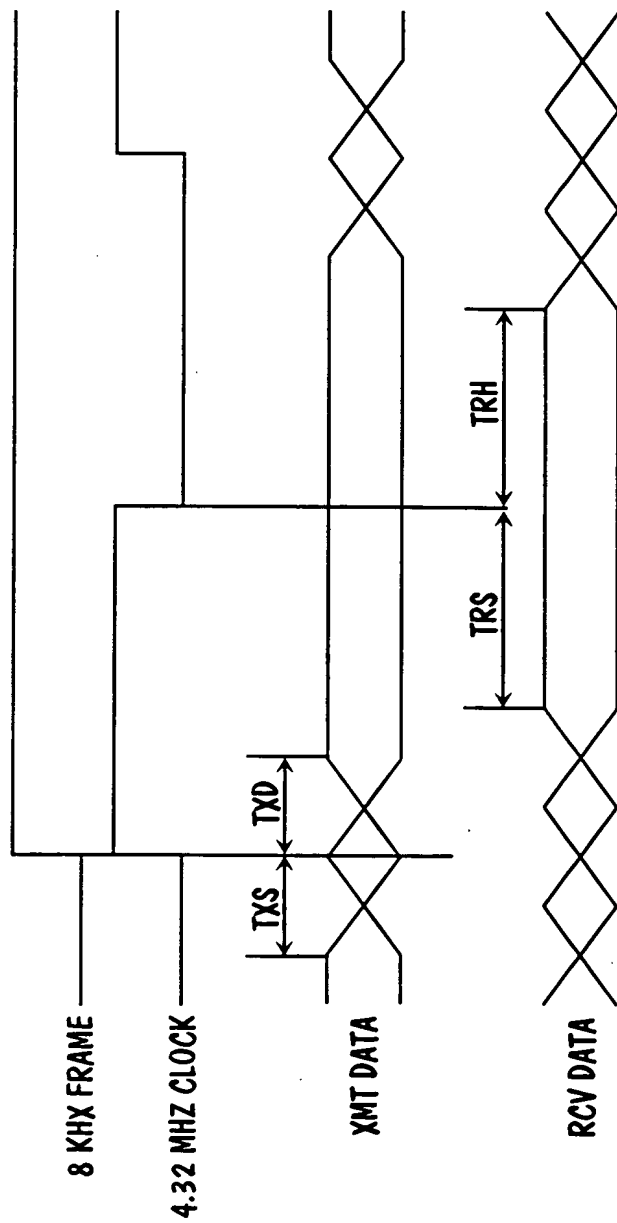


FIG. 20

005T60" T8929960

PARAMETER	DESCRIPTION	MIN	MAX
TXS	TRANSMIT SKEW		30 NSEC
TXD	TRANSMIT DELAY		60 NSEC
TRS	RECEIVE SETUP	30 NSEC	
TRH	RECEIVE HOLD	60 NSEC	

FIG. 21

005160" T8929960

BYTE		POS.		POS.		POS.	
0	K1 PORT 1	1	K2 PORT 1	2	K1 PORT 2	3	K2 PORT 2
4	K1 PORT 3	5	K2 PORT 3	6	K1 PORT 4	7	K2 PORT 4
8	K1 PORT 5	9	K2 PORT 5	10	K1 PORT 6	11	K2 PORT 6
12	K1 PORT 7	13	K2 PORT 7	14	K1 PORT 8	15	K2 PORT 8
16	K1 PORT 9	17	K2 PORT 9	18	K1 PORT 10	19	K2 PORT 10
20	K1 PORT 11	21	K2 PORT 11	22	K1 PORT 12	23	K2 PORT 12
24	K1 PORT 13	25	K2 PORT 13	26	K1 PORT 14	27	K2 PORT 14
28	K1 PORT 15	29	K2 PORT 15	30	K1 PORT 16	31	K2 PORT 16
32	E1 PORT 1	33	F1 PORT 1	34	SPARE	35	SPARE
36	SPARE	37	SPARE	38	SPARE	39	SPARE
40	SPARE	41	SPARE	42	SPARE	43	SPARE
44	SPARE	45	SPARE	46	SPARE	47	SPARE
48	SPARE	49	SPARE	50	SPARE	51	SPARE
52	SPARE	53	SPARE	54	SPARE	55	SPARE
56	SPARE	57	SPARE	58	SPARE	59	SPARE
60	SPARE	61	SPARE	62	SPARE	63	SPARE

FIG. 22

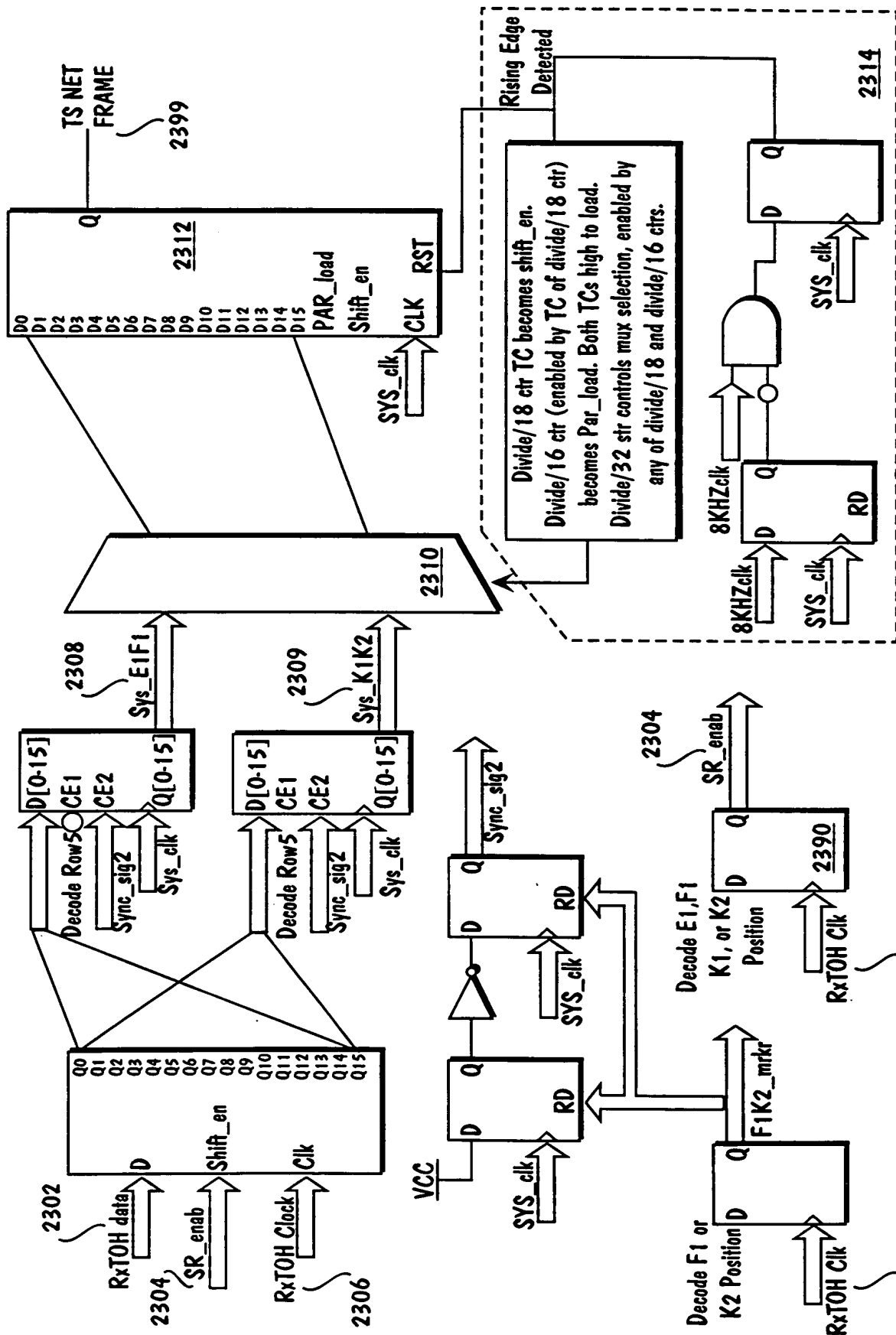


FIG. 23

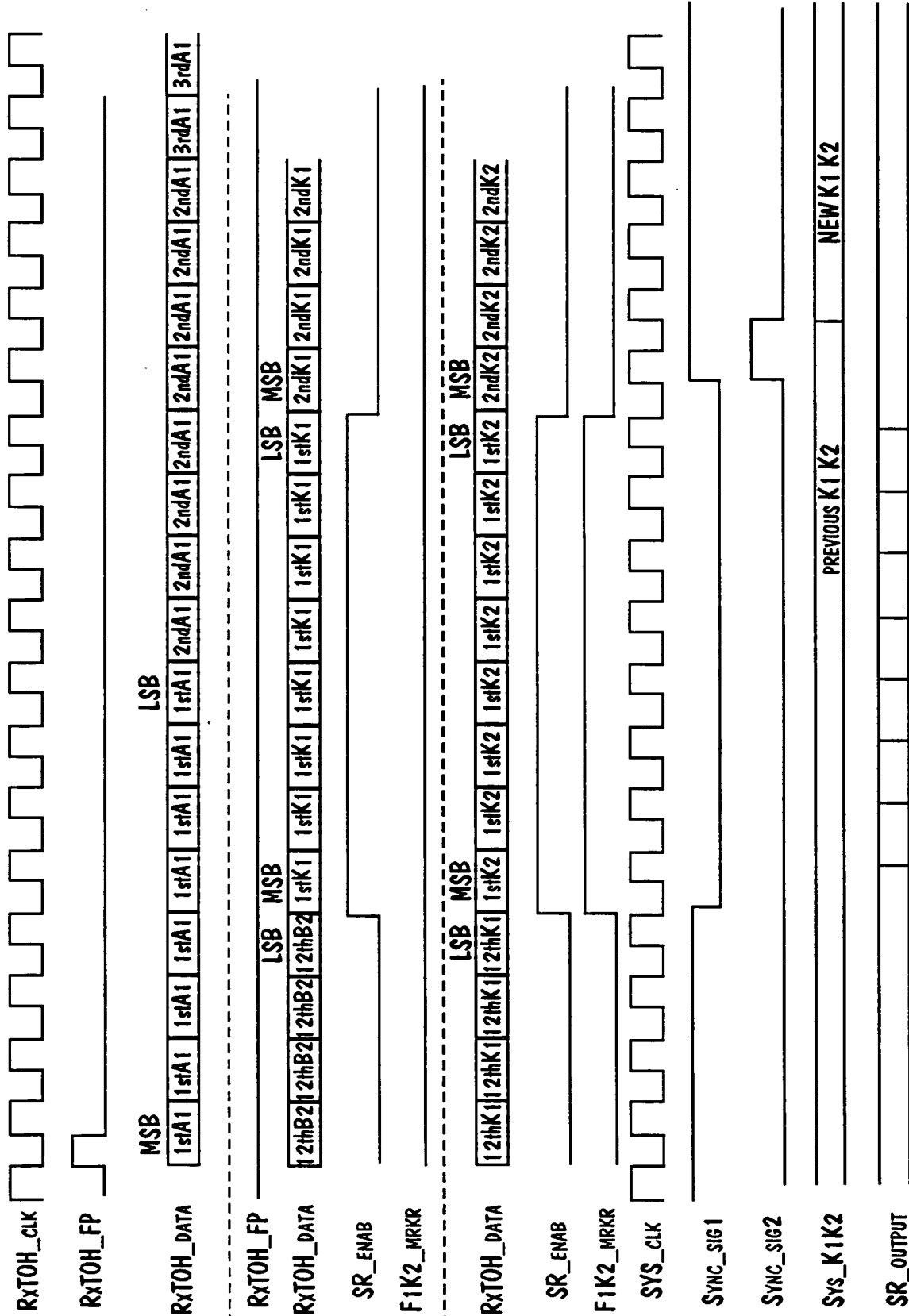


FIG. 24

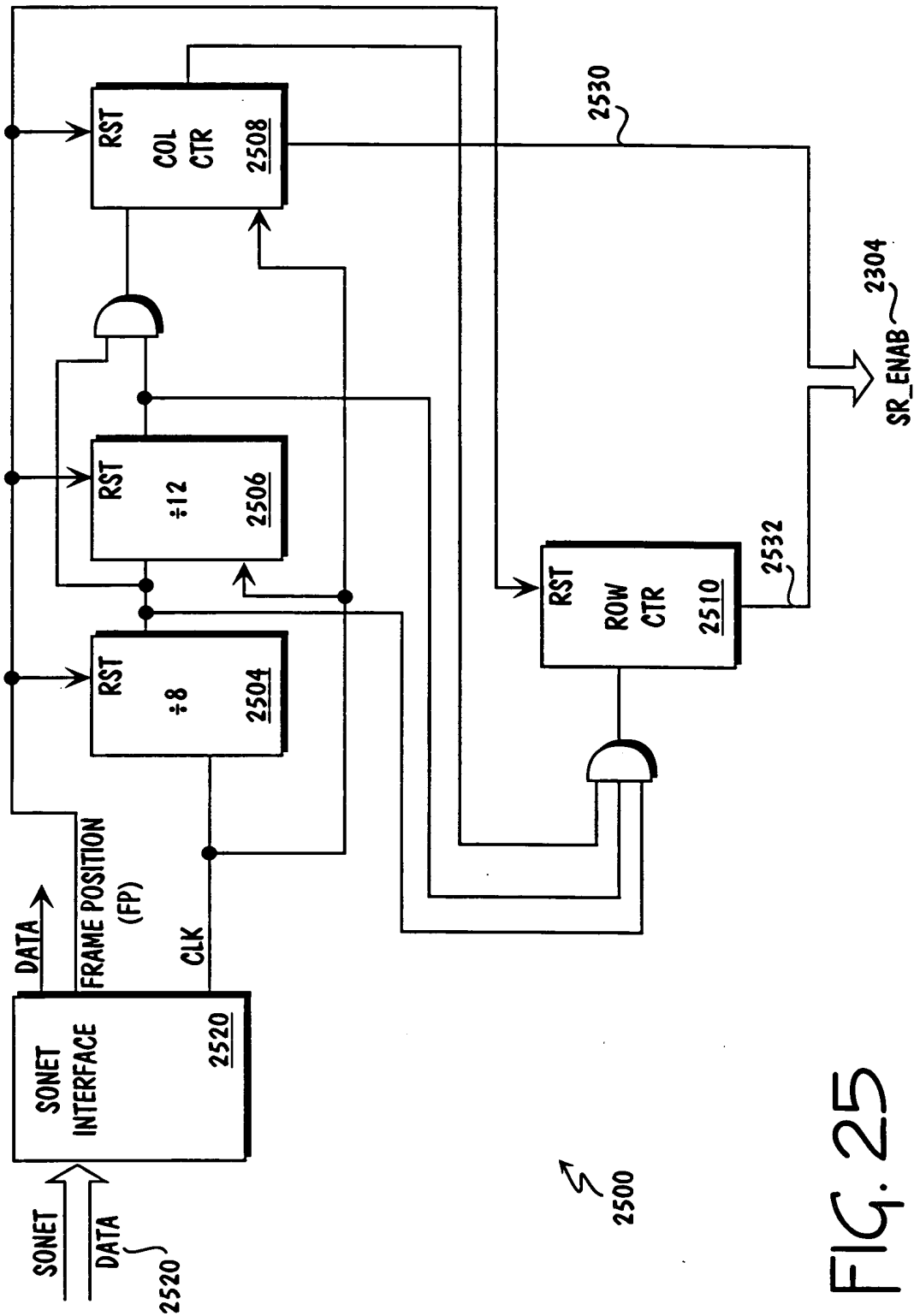


FIG. 25

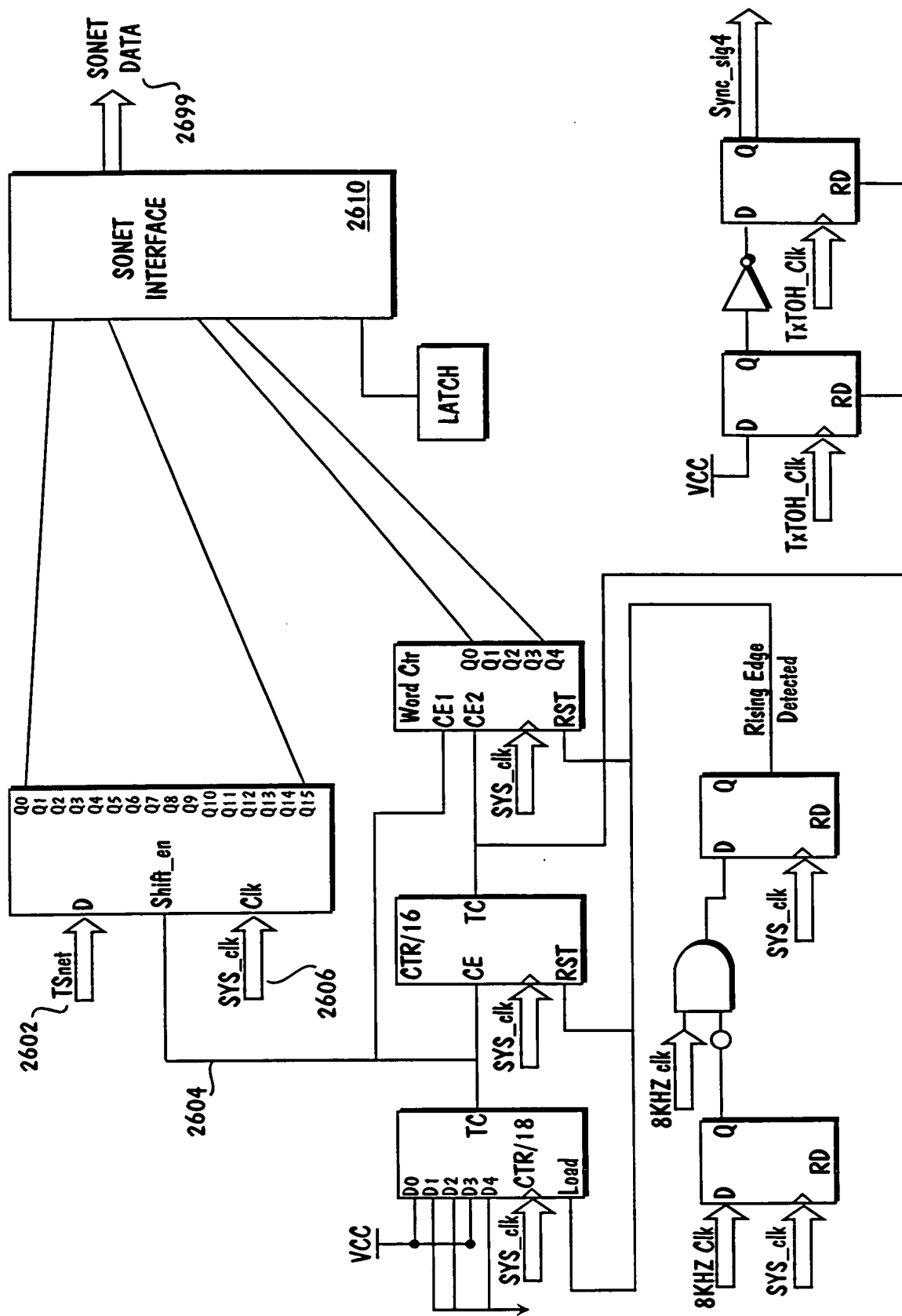


FIG. 26

09662681.091500

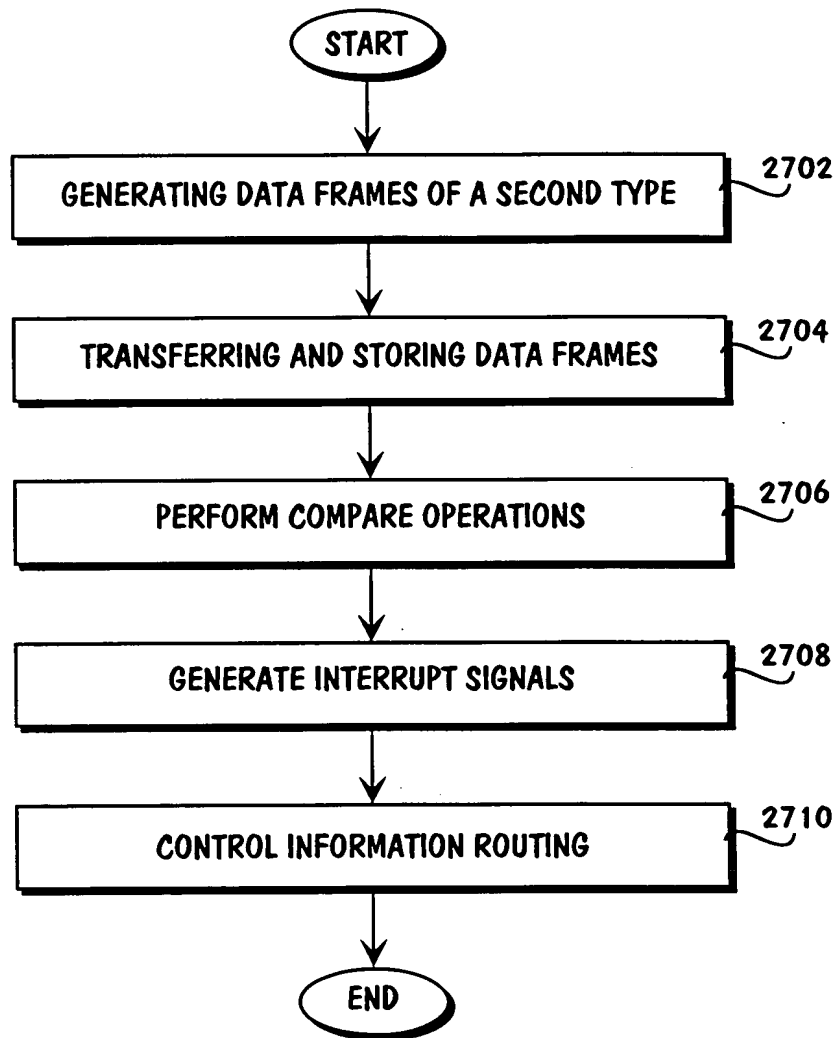


FIG. 27

09662681.091500

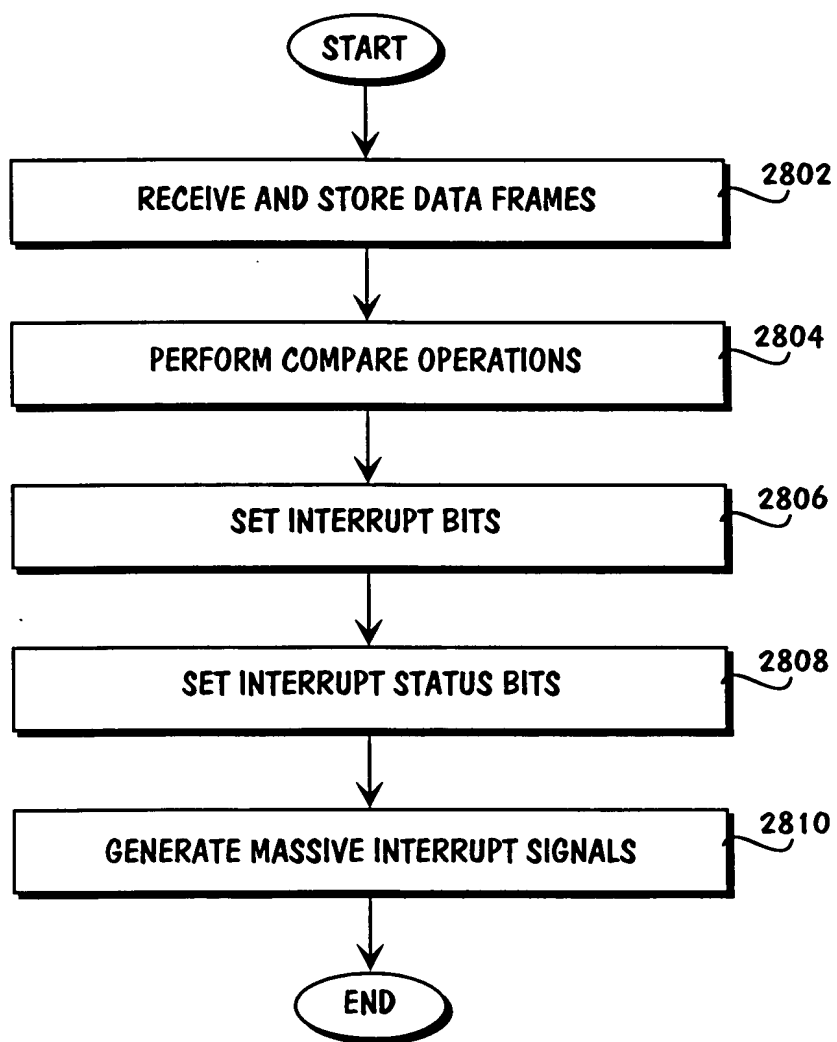


FIG. 28

005760 1892960 0962681 091500

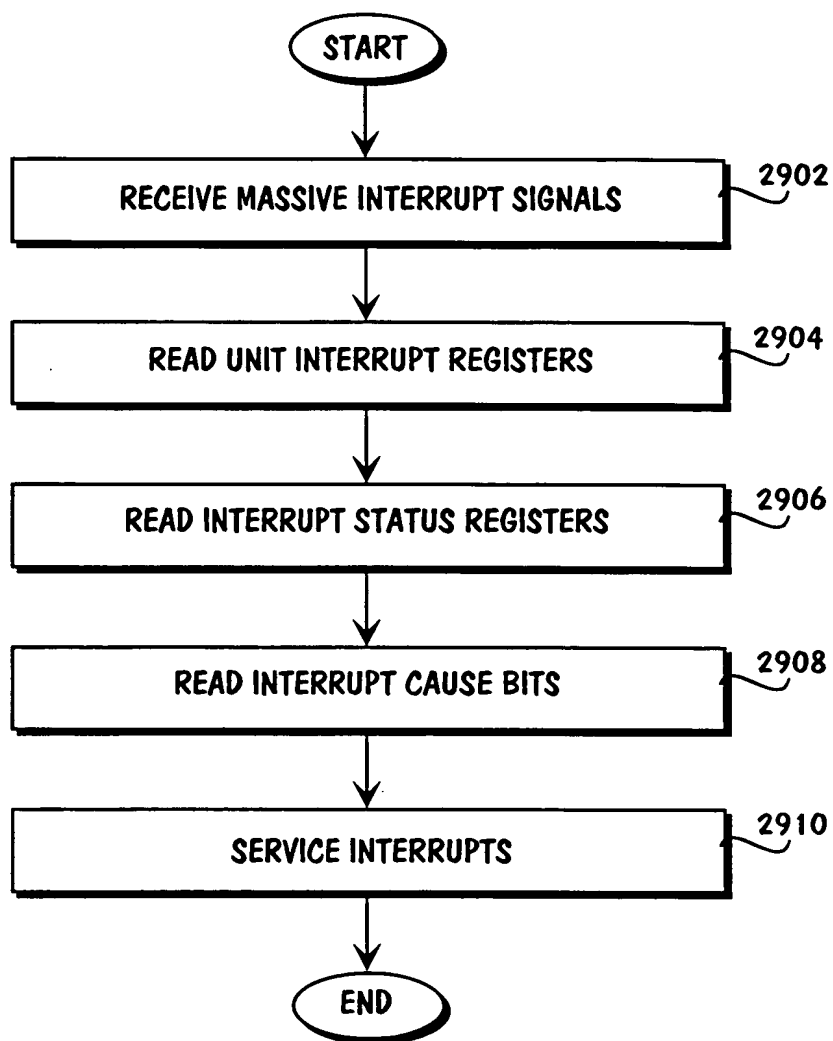


FIG. 29